d) reading the encoded digital video bit stream out of the encoder buffer at the second bit rate; and transmitting the encoded digital video bit stream to a decoder at the second bit rate.

5. (Four Times Amended) A video signal encoding apparatus for encoding a received digital video signal for transmission, the apparatus comprising:

an encoder stage for encoding a received video signal according to a predetermined coding algorithm and producing the encoded video signal as a variable bit-rate data stream at an output of said encoder stage;

a buffer coupled to receive said variable bit-rate data stream from the encoder stage and arranged to output a data signal corresponding thereto for transmission; and

means coupled to said encoder stage to (i) detect the bit-rate of said variable bit-rate data stream, (ii) derive a second bit rate as a percentage of the detected bit-rate, which percentage changes in inverse relation to changes in the detected bit-rate, [and] (iii) control said buffer to produce said output data signal at said second bit rate, and (iv) transmit the output data signal to a decoder at the second bit rate; wherein the detected bit-rate and said second bit rate are variable.

REMARKS

This Response is being filed in response to the outstanding Office Action dated December 10, 1997 wherein all the pending

claims have been rejected. A petition for one month extension of time is being filed concurrently herewith. Reconsideration and allowance of the application in view of the amendments made above and remarks to follow is earnestly requested.

Applicant takes this opportunity to highlight the feature which distinguishes the claimed invention from the cited prior art. The present invention is directed to a method of and apparatus for the transmission of encoded digital video signals. As amended, the claimed invention more particularly recites that the digital video bit stream, having been sequentially written into the encoder buffer at a first bit rate, is read out of the encoder buffer at the claimed second bit rate and is transmitted to a decoder buffer at the second bit rate. Accordingly, the present invention can achieve a substantially constant buffer fullness. Although prior art devices may avoid buffer overflow and underflow, they do so in a vastly different manner. That is, Applicant respectfully submits that the claimed invention is neither described nor suggested in the cited prior art.

For example, claims 1-12 and 14 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,606,369 ("Egawa"). Applicant respectfully traverses this rejection.

Firstly, although Egawa is directed to a method of avoiding data loss when an combined image is reproduced, Egawa does so in a patentably different manner from Applicant. In order to allow another sequence to be inserted in a main sequence, Egawa describes analyzing the sequences to determine a number of <u>stuffing</u> bits to insert in the data stream before the inserted sequence. The number

of stuffing bits to be inserted is based in part on the data rates of the main and inserted sequences. Thereafter, the stuffing bits are inserted after the selected splice point and before the inserted sequence. By controlling the insertion of the stuffing bits, Egawa may effectively control the encoder buffer fullness. However, Applicant respectfully submits that nowhere in the Egawa patent is there is description of writing a video signal bit stream into the encoder buffer at a first rate and transmitting the signal to a decoder at the claimed second bit rate.

In contra distinction thereto, Egawa merely describes the respective filling and emptying of encoder buffers 414 and 416. However, Applicant respectfully submits that nowhere is there a description of any one data stream being inputted to, for example, buffer 416, at a first rate and outputted to the decoder at a second rate. In particular, buffer 414 is used to gather information from which the value NSTUFF is calculated while the splicing is performed using buffer 416. This spliced signal is then transmitted from buffer 416 to buffer 424 of the decoder 420. At best, Applicant respectfully submits that Egawa describes the ability to transmit video signal portions to buffer 416 at different bit rates (see for example, col. 7, lines 16-37, which describe how a portion of STREAM2 is transmitted to buffer 416 at either bit rate R1 or R2). That is, Applicant respectfully submits that nowhere in the Egawa patent, even after reviewing the portion of column 8 cited by the Examiner, is there a description of the transmission of the data to the decoder at the respective inversely proportional data rates, as claimed.

For all of these reasons, Applicant respectfully submits that Egawa does not anticipate the invention as now claimed in independent claims 1 and 5, nor does Egawa anticipate independent claim 12, as discussed above, because Egawa does not maintain the constant buffer fullness as claimed, but rather, does so using the aforementioned stuffing bits. Accordingly, notice to the effect that claims 1-12 and 14 are patentable over Egawa is respectfully requested.

Secondly, claims 1, 5 and 12 are rejected on the basis of nonstatutory double patenting in view of U.S. Patent No. 5,606,369 ("Keesman"). Applicant respectfully traverses this rejection.

Specifically, the Examiner deems it would have been obvious for one of ordinary skill in the art to observe that the operation of the apparatus of claim 3 of Keesman in the presence of only a single encoder stage and single input channel would read on the apparatus of claim 5 because it also uses the same output bit-rate determination means of the apparatus as in claim 5. Applicant respectfully disagrees.

Applicant respectfully submits that the target setting unit 14 of Keesman is provided to assign global targets to individual video frames specifying the number of bits that the encoder must use in compressing the frame. On the other hand, it is the calculation stage 20, which is described as the unit that derives the values for the respective channel output bit rates from the buffer 16. Accordingly, although there in fact may be only a single encoder stage in the instant application, that does necessarily result in that the additional feature of the described target setting means

would be obvious in view of the claims of the instant application. Accordingly, reconsideration and removal of the double patenting rejection is most respectfully requested.

Applicant has made a sincere and diligent effort to place this application in condition for an immediate notice of allowance and notice to this effect is earnestly solicited.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited this date with the United States Postal Service as first class mail in an envelope addressed to:

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

Date: April 9, 1998

By: Arthur Schaier

Respectfully submitted,

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